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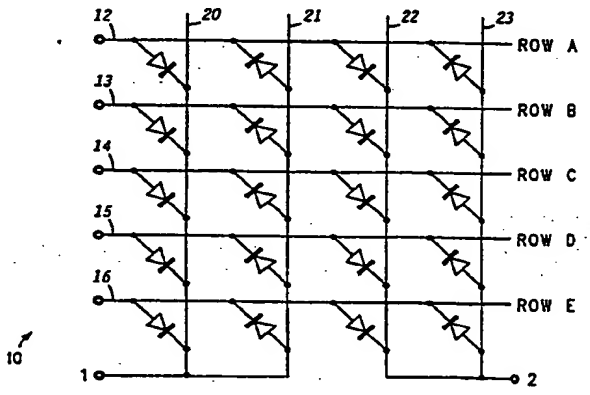
(54) Push-pull matrix addressing.

(57) A plurality of light emitting diodes (60) each diode including an anode (64) and a cathode (63), and divide into rows and columns. Rows and columns of conductors (62, 65) positioned to correspond, one each, with the rows and columns of diodes, and alternate columns of anodes and cathodes being reversed. Each row conductor has alternate cathodes and anodes connected thereto, and each column conductor with anodes connected thereto is connected to a column conductor with cathodes connected thereto so as to reduce the number of inputs by one half. A specific column of each pair is addressed by applying a positive or negative signal (b_0) to each input.

FIG. 2



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The present invention pertains to the addressing of matrixes and more specifically to matrixes and driving circuitry with reduced connections.

Background of the Invention

A matrix type array of components is utilized in a variety of electronic devices, such as displays and memories. In a matrix type array, the components are arranged into rows and columns with each row and each column having a separate input. To address a particular component, the row and column containing the component is energized. Thus, the specific component at the junction of the row and column, which is the selected component, is the only component that receives the correct energization to cause the component to be turned on.

The major problem with the matrix type array of components is the large number of external pads, or input terminals, that must be provided. Each row and each column has an individual, separate external pad. When the matrix type array being utilized has a large number of rows and columns, the number of external pads which are required becomes almost prohibitive. For example, in a matrix array of light emitting diodes (LEDs) utilized in a display, the number of rows could be 128 and the number of columns could be 240. This means 128 + 240 = 368 connections must be made to external control circuitry. The LEDs are generally fabricated on a GaAs substrate with a pitch of approximately 20 microns. In this specific instance the area of the LED matrix type array is 4.8 X 2.56 mils without the interconnects. The addition of 368 external pads increases the array area by a factor of approximately 2.3, which significantly increases the cost of the array. Further, the large number of connections to the array makes manufacturability of a complete display module difficult and reduces reliability of the finished product.

Summary of the Invention

It is a purpose of the present invention to provide a matrix type array which reduces the number of external pads or connections.

It is a further purpose of the present invention to provide a matrix type array which reduces the number of external connections without substantially increasing the cost of manufacture or the complexity.

It is a further purpose of the present invention to provide a matrix type array which reduces the number of external connections without requiring additional bus lines or substantially increasing the cost or complexity of the external drive circuitry.

The above described problems and others and the above purposes and others are realized in a push-pull addressable matrix including a substrate, a plurality of electrical components formed on the substrate, each component including a first and a second electrode, and the components being divide into rows and columns, and rows and columns of connecting conductors positioned on the substrate to correspond, one each, with the rows and columns of components and to couple to each first and second electrode of the components to provide an addressable matrix, with all of the first electrodes in each alternate column of the plurality of components being connected to a corresponding alternate column of the connecting conductors and all of the second electrodes of each interspersed column of the plurality of components being connected to the corresponding interspersed column of the connecting conductors, each of the remaining first and second electrodes being connected to a corresponding row of connecting conductors, and each alternate column of connecting conductors being connected to a different interspersed column of connecting conductors.

Brief Description of the Drawings

Referring to the drawings:

FIG. 1 illustrates a schematic diagram of a prior art matrix;

FIG. 2 illustrates a schematic diagram of a push-pull matrix of light emitting diodes incorporating a portion of the present invention;

FIG. 3 is a simplified cross-sectional view of a pair of LEDs connected as illustrated in FIG. 2;

FIG. 4 is a block diagram of a portion of a driving circuit for the matrix of FIG. 2;

FIG. 5 is another portion of a driving circuit for the matrix of FIG. 2; and

FIG. 6 illustrates an electronic communication device including a simplified block diagram of a complete driving circuit for the matrix of FIG. 2 to provide a complete display.

Description of the Preferred Embodiment

Referring specifically to FIG. 1, a matrix type array of diodes, constructed in accordance with the prior art, is illustrated. In this array, the diodes are arranged in rows and columns, with all of the anodes of the diodes in each row being connected together and all of the cathodes of the diodes in each column connected together. In the matrix illustrated there are five rows and four columns with each row and each column having an external connecting pad, for a total of nine external connecting pads. Nine external connecting pads are necessary to address each diode in the array of diodes.

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To address a specific diode a negative signal is applied to the external connecting pad (column) which is connected to the cathode of the diode and a positive signal is applied to the external connecting pad (row) which is connected to the anode of the diode. In this fashion the specific diode selected conducts and all other diodes are non-conducting.

Referring specifically to FIG. 2, a push-pull matrix 10 of light emitting diodes is illustrated. Matrix 10 includes twenty light emitting diodes formed on a single substrate and arranged into five rows and four columns. Rows of connecting conductors, designated 12 - 16, are positioned on the substrate to correspond, one each, with the diode rows and columns of connecting conductors, designated 20 - 23, are positioned on the substrate to correspond, one each, with the diode columns. The connecting conductors are couple to each anode and cathode of the diodes to provide addressable matrix 10, with all alternate columns of diodes being reverse connected. Thus, all of the diodes in alternate columns have a cathode connected to the column conductor, i.e. conductors 20 and 22, and all of the diodes in interspersed columns have an anode connected to the column conductors, i.e.conductors 21 and 23. Similarly, in each row, the anode of alternate diodes is connected to the row conductor and the cathode of interspersed diodes is connected to the row conductor. Matrix 10 is designed for an LED display and, therefore, alternate columns of diodes are reverse connected, for reasons which will be apparent presently. It will of course be understood that in many applications it may be more convenient to reverse alternate rows of diodes and, therefore, the terms "row" and "column" are generally used interchangeably herein.

The reverse connected LEDs, as applied to an LED imaging matrix, is feasible because the LED imaging array is fabricated on a GaAs substrate with the diodes being internally reverse coupled while retaining an acceptable pitch. This embodiment results in an efficient internal interconnect which requires no additional devices on the LED array and very little additional work during fabrication of the array. Other embodiments exist but require additional devices which are difficult to fabricate and take up additional space.

Each of the row conductors 12 - 16 have an external connecting pad connected thereto. Each alternate column conductor is connected to an adjacent interspersed column conductor to form pairs of column conductors, 20, 21 and 22, 23. Each pair of column conductors has a single external connecting pad connected thereto. In push-pull matrix 10 there are only two external connecting pads to all four columns 20 - 23. Thus, in simplified push-pull matrix 10, the number of external connecting pads has been reduced from the traditional number of nine to only seven. It will be apparent to those skilled in the art that expanding push-pull matrix 10 to 128 rows and 240 columns will result in a total of 128 X 240/2 = 248 total external connections. Thus, the total number of external connections has been reduced by 120 external connections.

FIG. 3 is a simplified view in cross section of an embodiment of a pair of semiconductor/organic light emitting diodes 60 connected as described above. Diodes 60 are constructed by starting with an optically transparent substrate 61 formed of some convenient material such as glass. A layer 62 of optically transparent conductive material is deposited on the surface of substrate 61 to form a first electrical contact. In this specific embodiment layer 62 is formed of indium tin oxide. A carrier injection layer 63 of semiconductor material which is optically transparent is deposited on layer 62. A typical example of an optically transparent semiconductor material is diamond. Next a light emitting layer 64 of electroluminescent material is deposited on carrier injection layer 63. Finally, an electrically conductive layer 65 is deposited on light emitting layer 64 to form a second electrical contact. Since it is desirable that all light emitted by layer 64 be directed through layers 63, 62 and 61, layer 65 is any convenient metal.

Diodes 60 are patterned on substrate 61 so as to leave a space 66 therebetween. Layers 62 and 65 are formed to extend into space 66 a short distance and a vertical connection 67 is deposited in space 66 so as to internally connect opposite terminals of the diodes 60. Generally, vertical connection 67 can be formed with the deposition of layer 65. While a specific type of LED is utilized herein for illustrative purposes, it will be understood by those skilled in the art that other types of LEDs and electronic components can be utilized in a similar fashion. To provide the column connections described in conjunction with push-pull matrix 10, layer 62 is patterned to extend between all of the diodes in an alternate column and layer 65 is patterned to extend between all of the diodes in an interspersed column. Thus, all of the connections for the push-pull matrix are made internally with virtually no additional process steps

Referring specifically to FIG. 4, a column driving circuit 30 is illustrated, which is designed to be utilized with push-pull matrix 10. Column driving circuit 30 includes a counter 31 and a plurality of logic circuits 32, only one of which is illustrated. Each logic circuit 32 includes a first logic gate 33, a pair of logic gates 34 and 35 and P and N channel complementary drivers 36 and 37, respectively. In this specific embodiment, counter 31 is a nine bit counter, which may for example be a

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simple ripple counter. Also, in each logic circuit 32, first logic gate 33 is an eight input NAND gate, and logic gates 34 and 35 are two input NOR gates. Complementary drivers 36 and 37 are P and N channel FETs connected in series between a power source V_{DD} and a reference voltage, which in this instance is ground.

The first bit output of counter 31 is used as a polarity bit and is applied, in each logic circuit 32, directly to one input terminal of gate 35 and through an inverter to one input terminal of gate 34. The next eight output bits of counter 31 are applied, in each logic circuit 32, to the eight input terminals of gate 33. The eight input terminals are coded so that only one specific combination of output bits will cause gate 33, in each logic circuit 32, to produce an output. The coded connection to each gate 33 can be accomplished in a variety of ways, as for example inverting all inputs in the first logic circuit. In this fashion gate 33 of the first logic circuit would produce an output each time counter 31 produced the output 00000000. Similarly, gate 33 of the next logic circuit is coded so that an output is produced in response to the output 00000001 from counter 31, and so on.

The output terminal of gate 33 is connected directly to second input terminals of each of gates 34 and 35. An output terminal of gate 34 is inverted and applied to the control gate of driver 36 and an output terminal of gate 35 is applied directly to the control gate of driver 37. The junction of drivers 36 and 37, which is output terminal 38, is connected to the connecting pad of columns 20, 21 of push-pull matrix 10. In this specific embodiment, the first (least significant) output bit of counter 31 alternately selects gate 35 (a 0 output bit) and, on the next clock pulse, gate 34 (a 1 output bit). Further, the other eight output bits remain constant through this switching of the first bit, so that on the first two clock pulses applied to counter 31: first, driver 37 is activated to ground output terminal 38 and then driver 36 is activated to apply VDD to output terminal 38. Thus, column 20 of push-pull matrix 10 is addressed on the first clock pulse and column 21 is addressed on the second clock pulse. Because eight output bits of counter 31 are utilized to address the plurality of logic circuits 33, as many as 256 logic circuits can be individually addressed.

Referring specifically to FIG. 5, a single row driving circuit 40 is illustrated. A similar row driving circuit 40 is provided for each row connecting pad. Each row driving circuit 40 includes a pair of two input terminal gates 41 and 42, two P channel drivers 43 and 44 and two N channel drivers 45 and 46. The P channel drivers 43 and 44 are connected in series between power source V_{DD} and an output terminal 47. The N channel drivers 45 and 46 are connected in series between output terminal 45 and a reference potential, which in this embodiment is ground. P channel driver 43 and N channel driver 46 act as constant current sources and are activated by bias voltages applied to the control gates thereof. An output terminal of gate 41 is connected to the control gate of P channel driver 44 and an output terminal of gate 42 is connected to the control gate of N channel driver 45. One input terminal of each of gates 41 and 42 is connected to a data input terminal 48. The second input terminal of gate 41 is connected through an inverter to the first (least significant) output bit terminal of counter 31 and the second input terminal of gate 42 is connected directly to the first output bit terminal of counter 31.

In this embodiment, data on terminal 48 consists of a series of 1's and 0's which are indicative of whether a specific LED is to be activated or not. However, since the diodes in interspersed columns 21 and 23 are reverse connected, it is necessary to apply a potential to the rows which is lower than the potential applied to interspersed columns 21, 23 to activate these diodes. Also, for the alternate columns in which the diodes are not reverse connected, a positive potential must be applied to the selected rows to activate the diodes. Thus, when an alternate column 20 or 22 is selected by the first output bit of counter 31, the same output bit of counter 31 causes gates 41 and 42 of the row driver circuits to select P channel driver 44 which, if the current data bit is a 1, is turned on. Similarly, when an interspersed column 21 or 23 is selected by the first output bit of counter 31, the same output bit of counter 31 causes gates 41 and 42 of the row driver circuits to select N channel driver 45 which, if the current data bit is a 1, is turned on.

FIG. 6 illustrates an electronic communication device 49 including a simplified block diagram of a complete driving circuit 50 for the matrix of FIG. 2 to provide a complete display. Communications device 49 is any device which might incorporate a display for displaying messages to be sent and/or received, for example a two way radio or pager. Driving circuit 50 includes counter 31, a plurality of logic circuits 32, a plurality of row driving circuits 40 and a random access memory (RAM) 52 connected to receive video data from an external interface. Counter 31 supplies the polarity bit and the eight bit address to each of the plurality of logic circuits 32, as described above. Thus, each of the columns is sequentially addressed. Counter 31 also supplies the polarity bit to each of the plurality of row drivers 40 and clocks RAM 52 so that data bits are supplied to the plurality of row drivers 40 in synchronism with the address inputs and polarity bit supplied to logic circuits 32 and row drivers 40.

The number of external connections, or connecting pads, required to address the columns in

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the matrix is reduced by one-half. Further, reversing the connections to interspersed columns is accomplished internally while manufacturing the matrix so that no additional space and virtually no additional processing steps are required. Also, the internal connections do not require additional devices on the array. The push-pull matrix requires no additional complicated driving circuits, or additional bus lines in the driving circuits, or expensive external circuitry. The simplicity of the driving circuits is illustrated in the disclosed driving circuits. While specific driving circuits have been disclosed which incorporate the speed and convenience of CMOS circuits, it will be understood that other driving circuits utilizing different conductivity types, etc. may be devised.

Claims

1. A push-pull addressable matrix including a substrate (61) and a plurality of electrical components (60) formed on the substrate, each component including a first and a second electrode (63, 64), and the components being divide into rows and columns, the matrix being characterized by:

   rows and columns of connecting conductors (62, 65) positioned on the substrate to correspond, one each, with the rows and columns of components and to couple to each first and second electrode of the components to provide an addressable matrix, with all of the first electrodes in each alternate column of the plurality of components being connected to a corresponding alternate column of the connecting conductors and all of the second electrodes of each interspersed column of the plurality of components being connected to the corresponding interspersed column of the connecting conductors, and each of the remaining first and second electrodes being connected to a corresponding row of connecting conductors.

2. A push-pull addressable matrix as claimed in claim 1 further characterized in that each row of connecting conductors includes an external row connector and each alternate column is connected to an interspersed column and includes an external column connector.

3. A push-pull addressable matrix as claimed in claim 2 further characterized by a plurality of logic circuits (30), each logic circuit being constructed to selectively provide first and second output signals, each logic circuit being connected to supply the first and second output signals to a different one of the external column connectors, and each of the first and second output signals being formed to activate a different one of the alternate and interspersed columns.

4. A push-pull addressable matrix as claimed in claim 3 further characterized by a plurality of driver circuits (40), each driver circuit being constructed to selectively provide first and second output signals, each driver circuit being connected to supply the first and second output signals to a different one of the external row connectors, and each of the first and second output signals being formed to activate the electrical component attached to the different one of the external row connectors and in the activated different one of the alternate and interspersed columns.

5. A push-pull addressable matrix as claimed in claim 3 further characterized by a counter (31) having a plurality of multi-bit output terminals (b_1 - b_8) designed to provide a plurality of multi-bit output signals and a direction output terminal (b_0), and wherein the plurality of logic circuits are each coupled to receive the multi-bit output signals from the counter, with each output signal addressing a selected one of the plurality of logic circuits.

6. A push-pull addressable matrix as claimed in claim 5 further characterized in that each of the plurality of logic circuits includes a first logic gate (33) having multi-bit input terminals connected to the multi-bit output terminals (b_1 - b_8) of the counter (31) and an output terminal, the first logic gate of each of the plurality of logic circuits being designed so that each of the plurality of multi-bit output signals selects a different logic circuit to energize so as to produce an output signal on the output terminal.

7. A push-pull addressable matrix as claimed in claim 6 further characterized in that each of the logic circuits further includes a pair of logic gates (34, 35) connected to receive the output signal from the included first logic gate and a direction signal from the direction terminal (b_0) of the counter, the direction signal being connected to select a particular one of the pair of logic gates to energize in conjunction with the output signal from the included first logic gate.

8. A push-pull addressable matrix as claimed in claim 4 further characterized in that the driver circuits are further coupled to receive data signals representative of an illustration to be displayed.

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9. A push-pull addressable matrix as claimed in claim 1 further characterized by a memory (52) coupled to receive and store data signals, the memory being coupled to the driver circuits for supplying data signals thereto.

10. A push-pull addressable matrix as claimed in claim 6 further characterized by a communications device selected from one of a two way radio and a pager.

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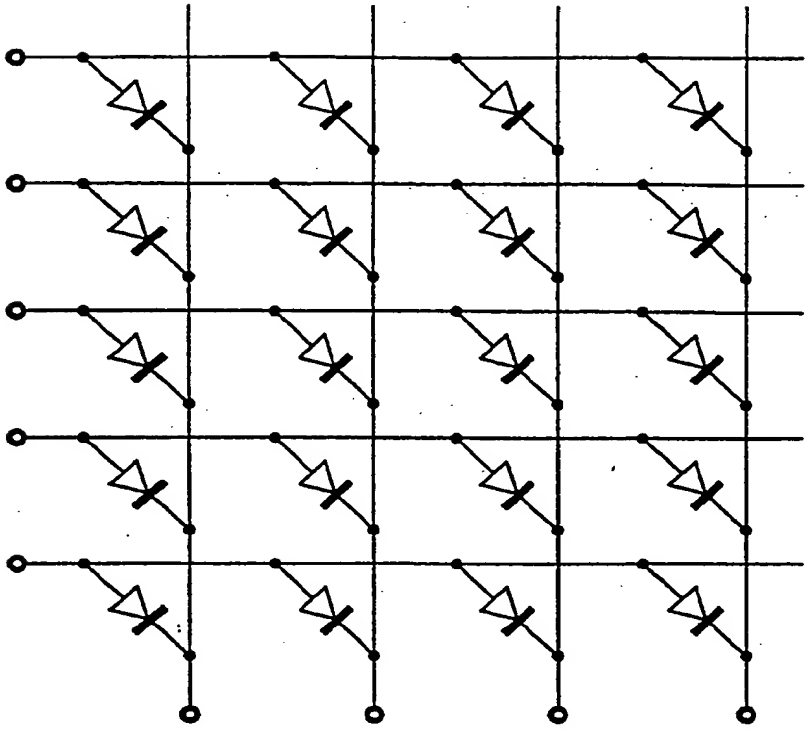
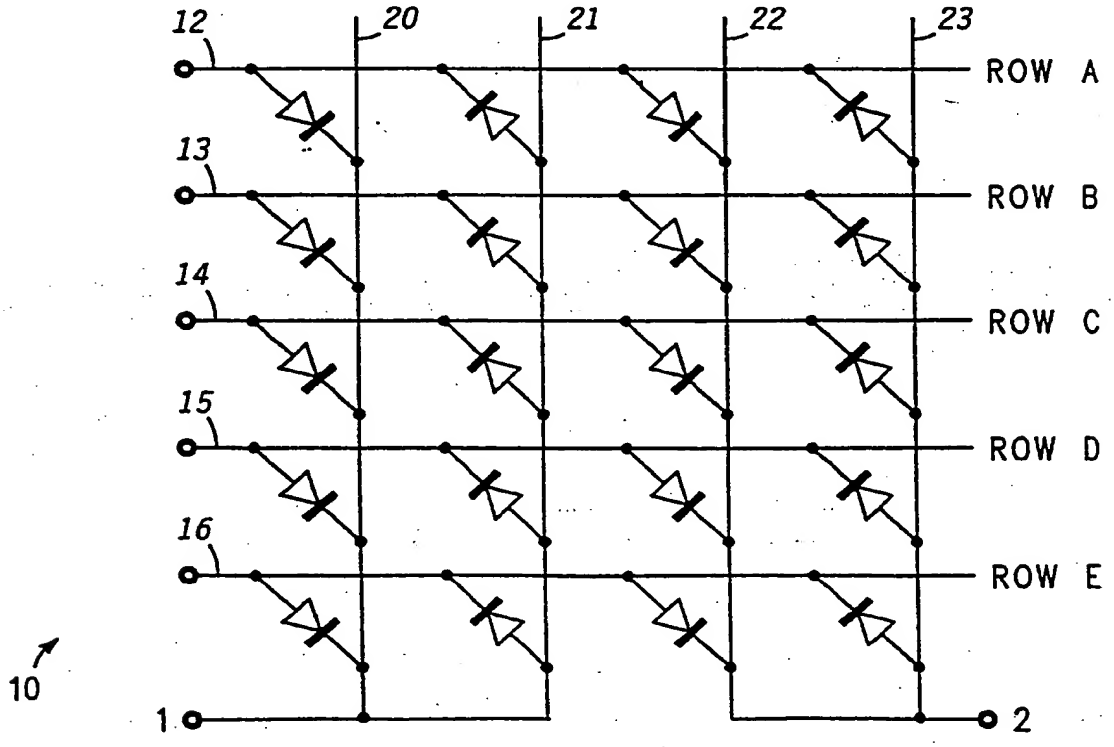


FIG. 1
-PRIOR ART-

FIG. 2



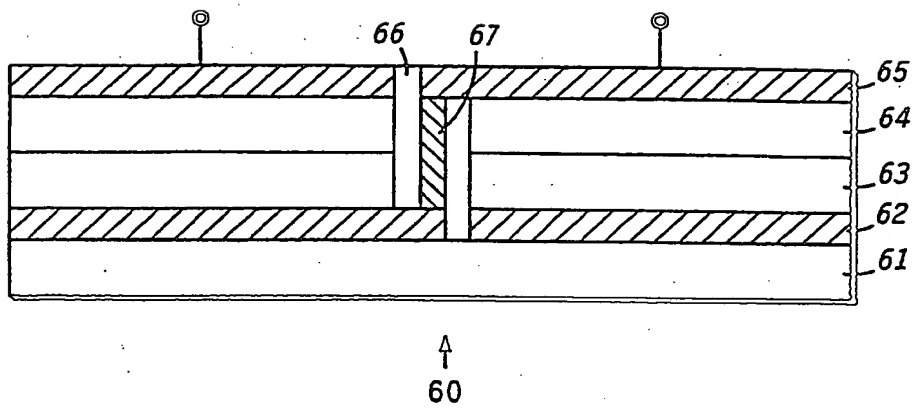
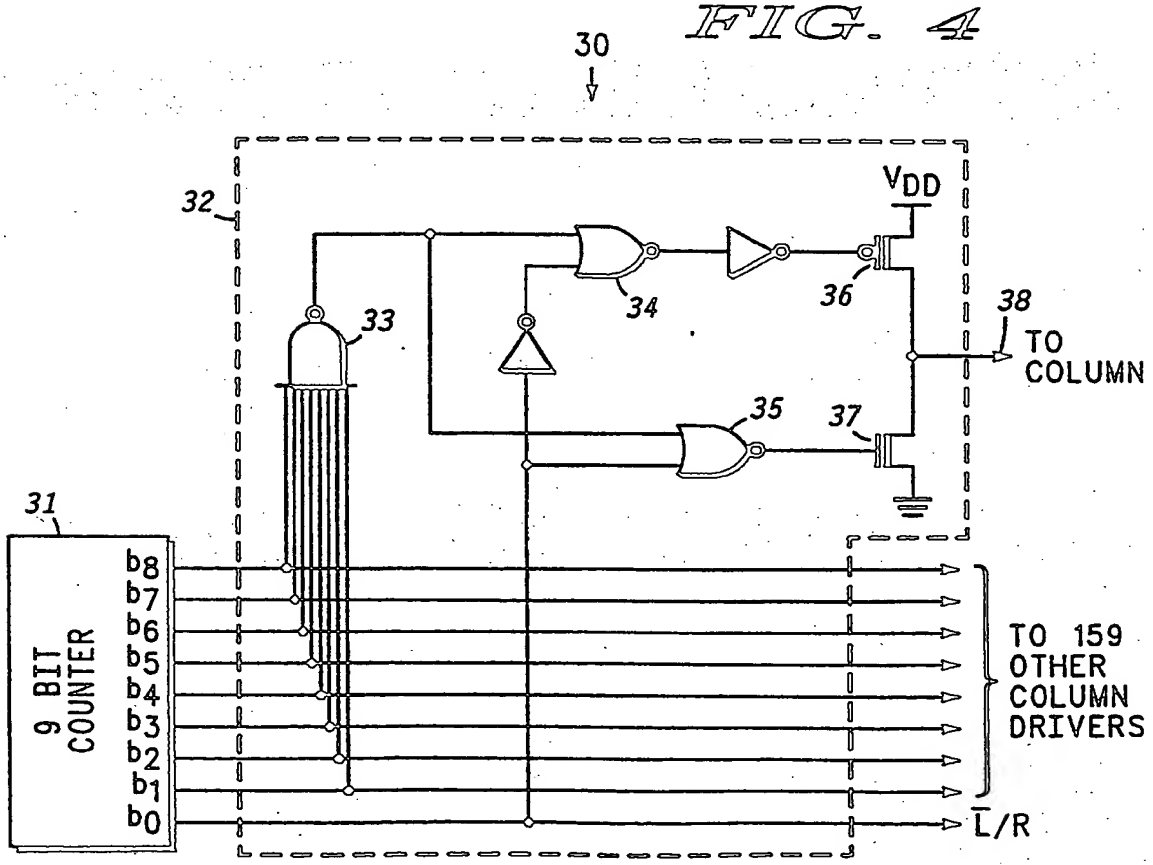

66
67
65
64
63
62
61
60

FIG. 3

FIG. 4


30
32
V_{DD}
33
34
36
38
TO COLUMN
35
37
31
9 BIT COUNTER
b_8
b_7
b_6
b_5
b_4
b_3
b_2
b_1
b_0
TO 159 OTHER COLUMN DRIVERS
$\overline{L}/R$

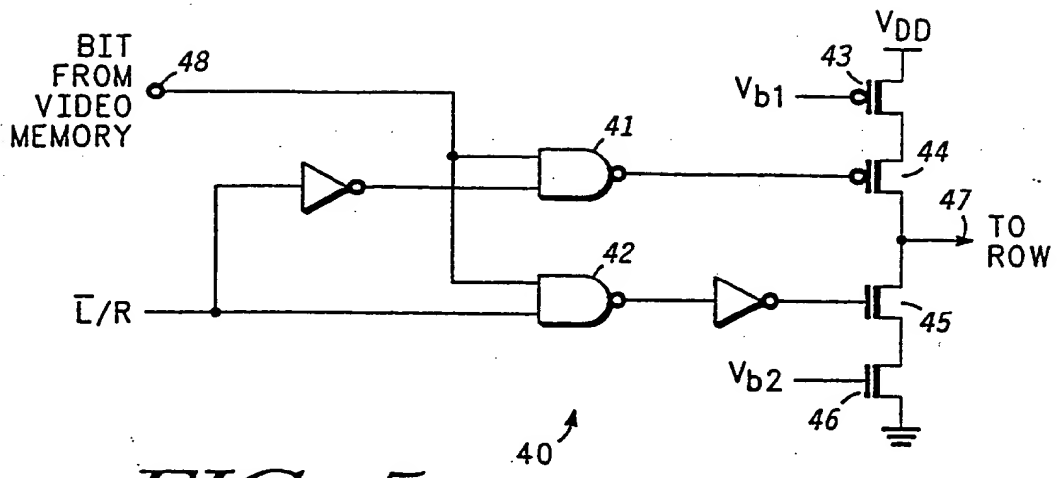
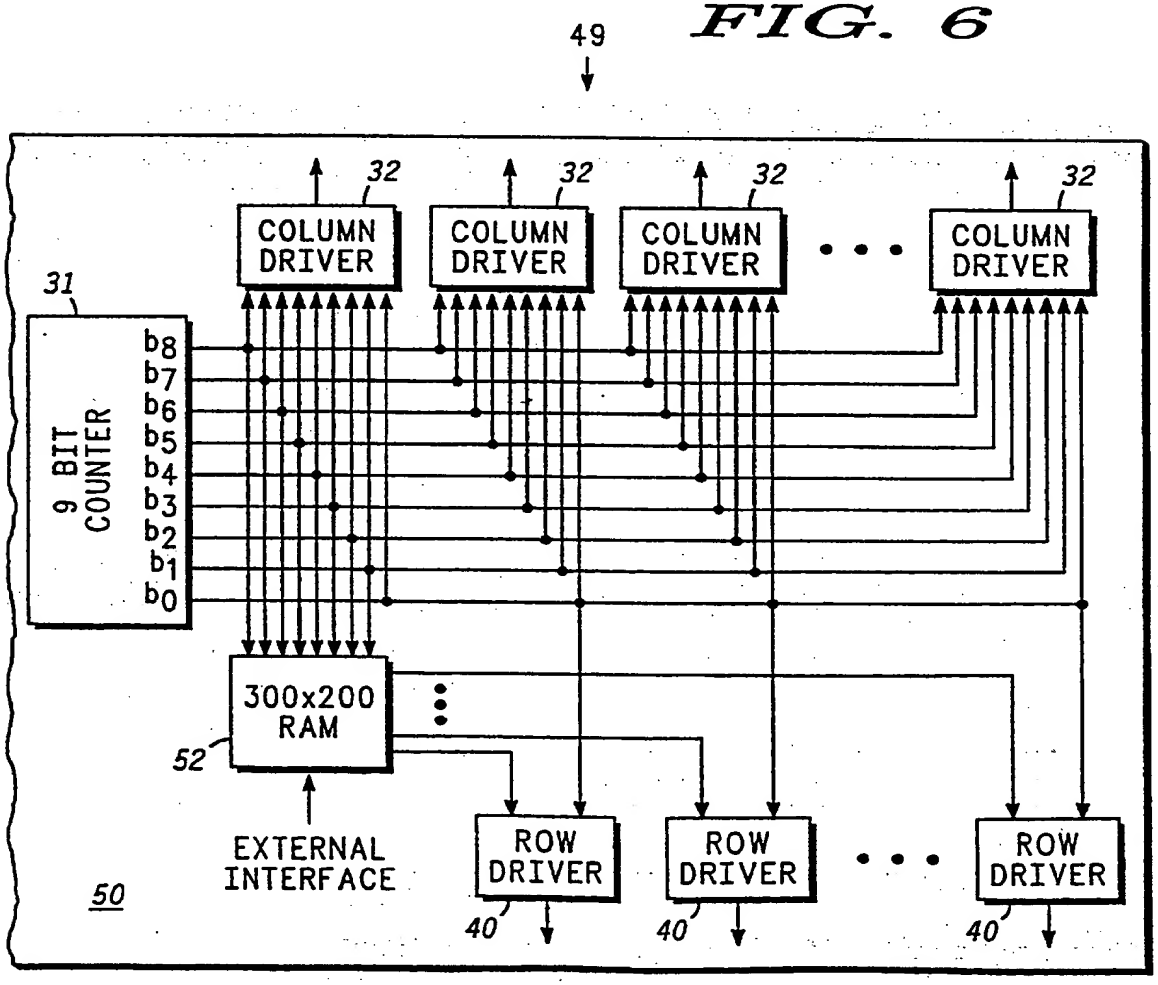

BIT FROM VIDEO MEMORY
48
V_{DD}
43
V_{b1}
41
44
47
TO ROW
42
$\overline{L}/R$
45
V_{b2}
46
40

FIG. 5

FIG. 6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b_7
b_6
b_5
b_4
b_3
b_2
b_1
b_0
300x200 RAM
52
EXTERNAL INTERFACE
50
ROW DRIVER
40

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 11 5480

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X A	US-A-3 696 393 (MCDONALD) * the whole document *	1,2 3,4	G09G3/32
A	FR-A-2 207 620 (THOMSON-CSF) * page 2, line 9 - line 30 * * page 4, line 28 - page 5, line 23 * * figures 1,2,4 *	1-4	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G09G
H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 March 1994	Farricella, L

CATEGORY OF CITED DOCUMENTS

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